

5749763

APPROVED	O.G. FIG.	
	CLASS	SUBCLASS
BY	CRAFTSMAN	

FIG.1

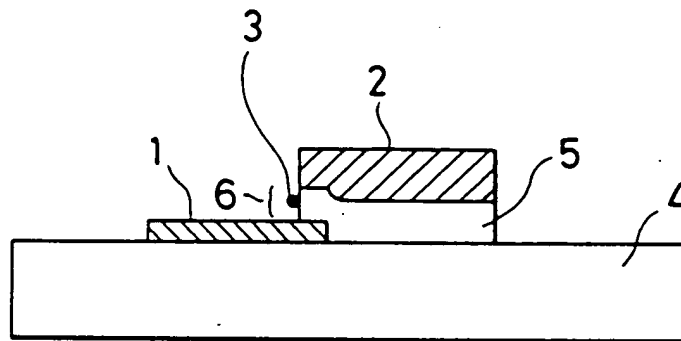
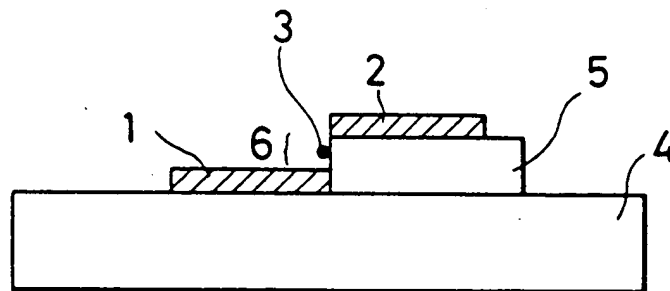


FIG.2



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FIG.3A

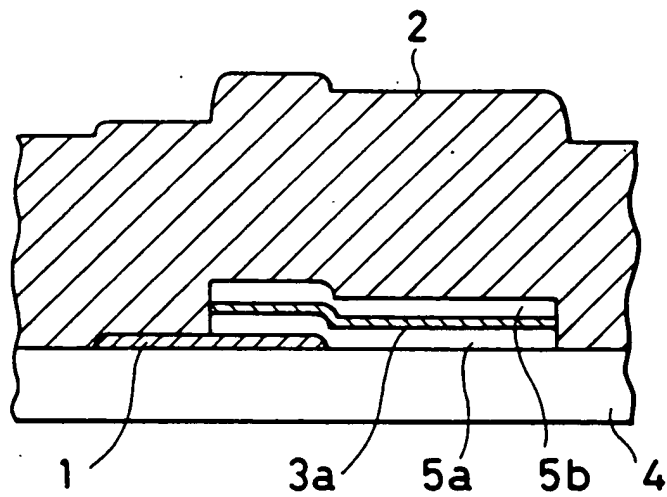
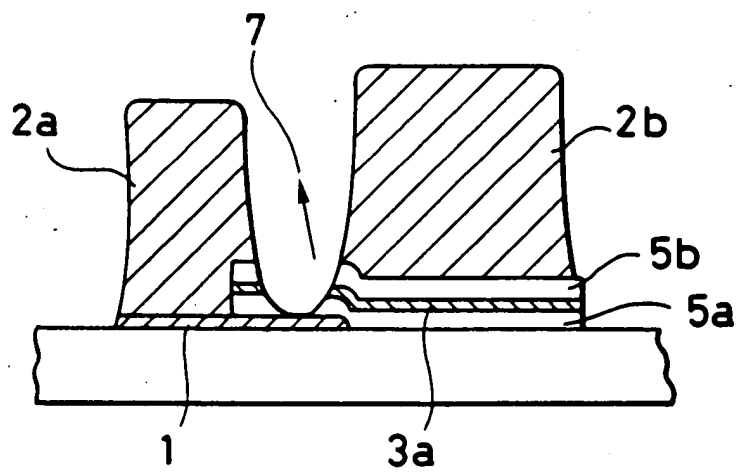


FIG.3B



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FIG.6A

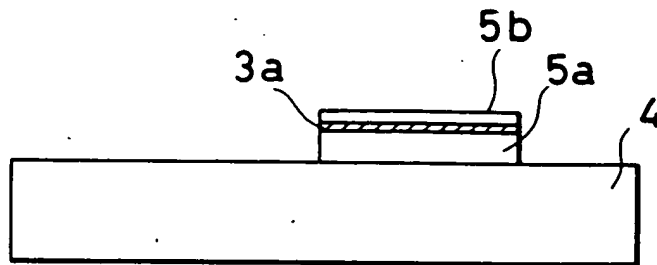


FIG.6B

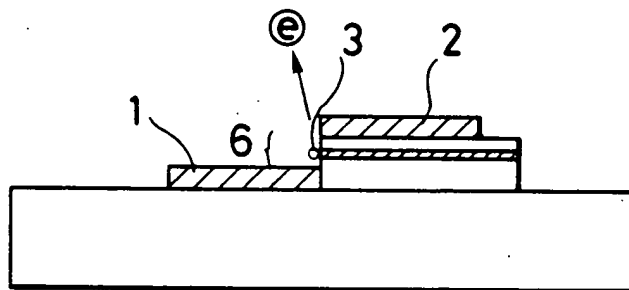
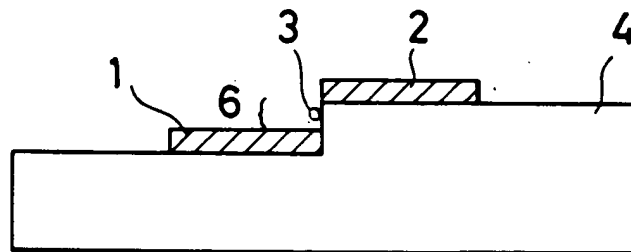


FIG.7



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FIG.8

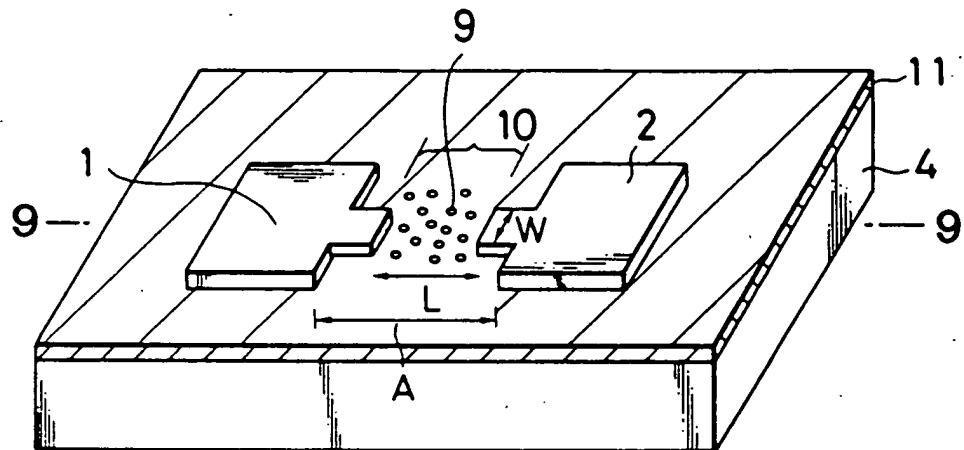


FIG.9

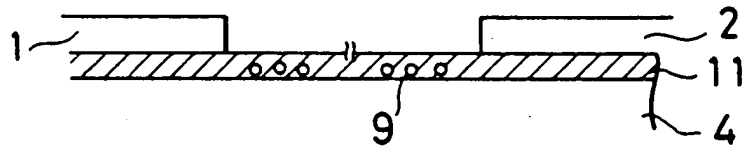
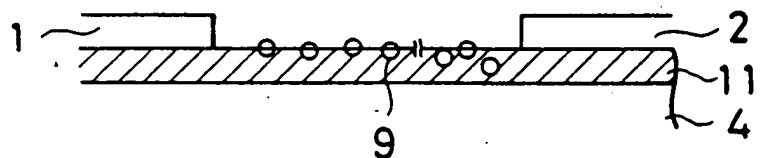


FIG.10



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FIG.12

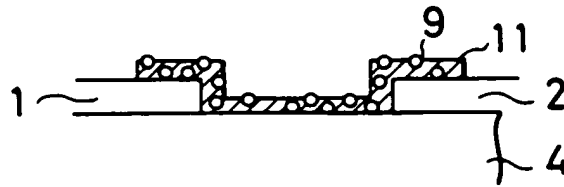


FIG.13A

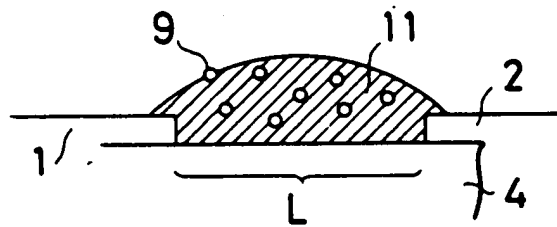
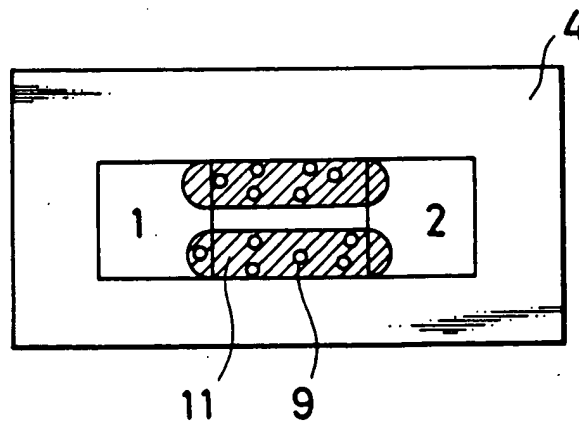


FIG.13B



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FIG.16A

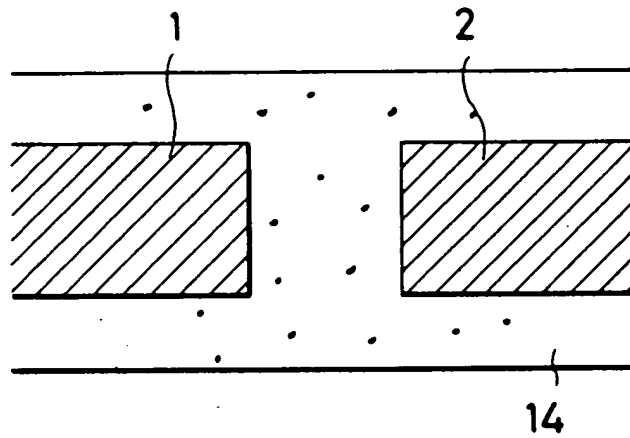
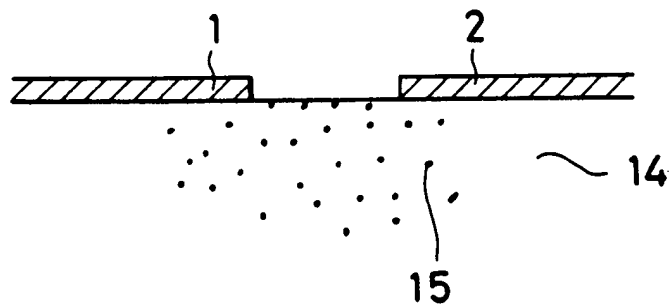


FIG.16B



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FIG.17

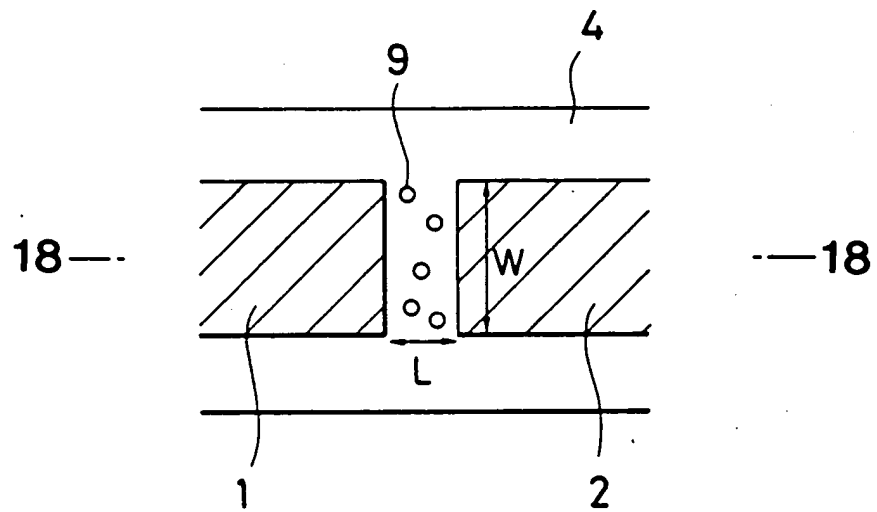
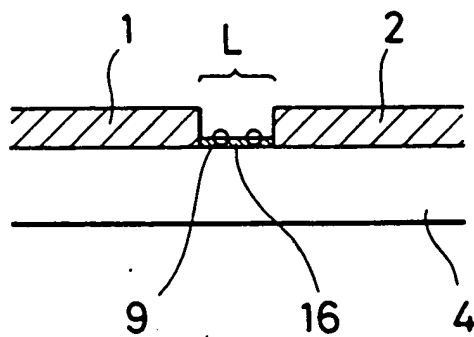
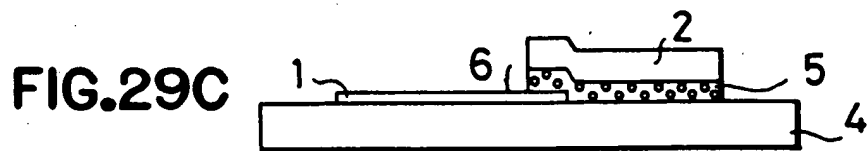
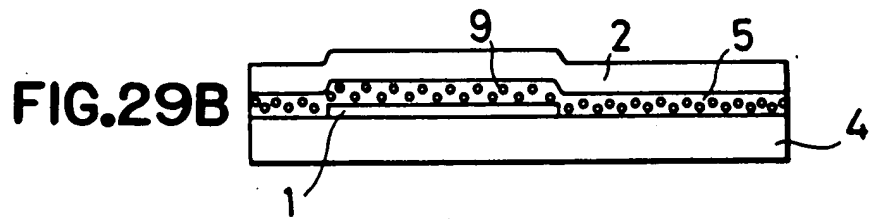
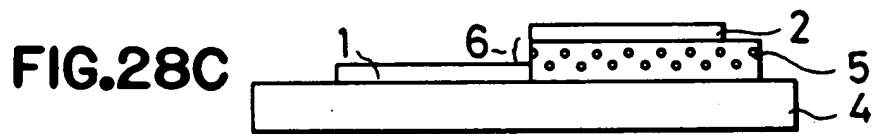
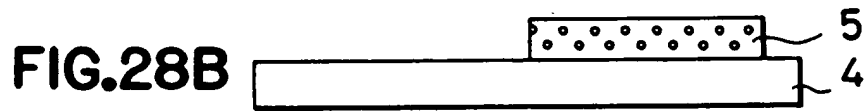
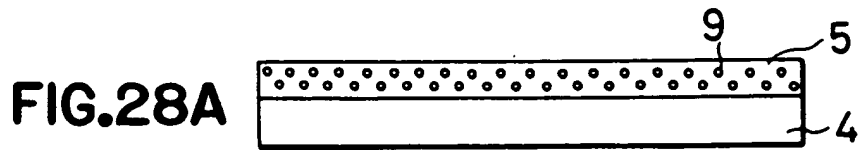


FIG.18



APPROVED	O.G. FIG.	
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APPROVED	O.G. FIG.	
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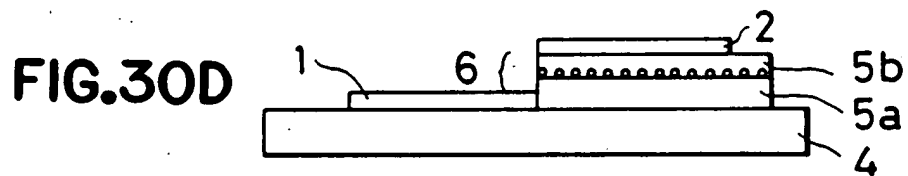
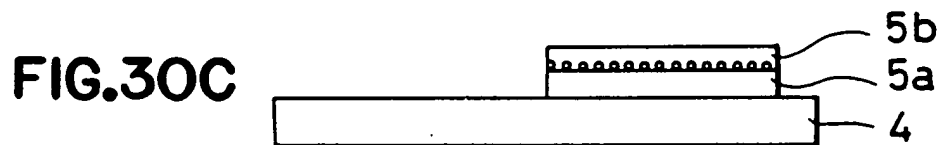
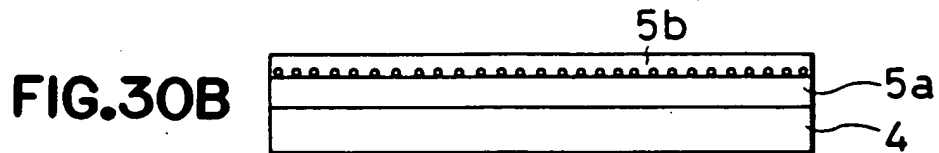
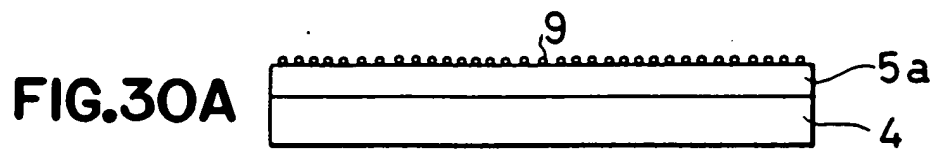
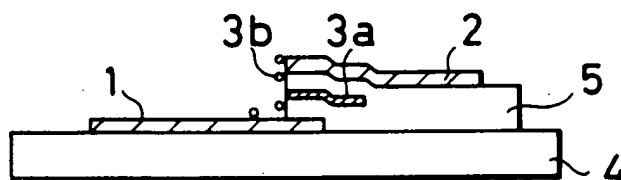


FIG.31



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FIG.32A

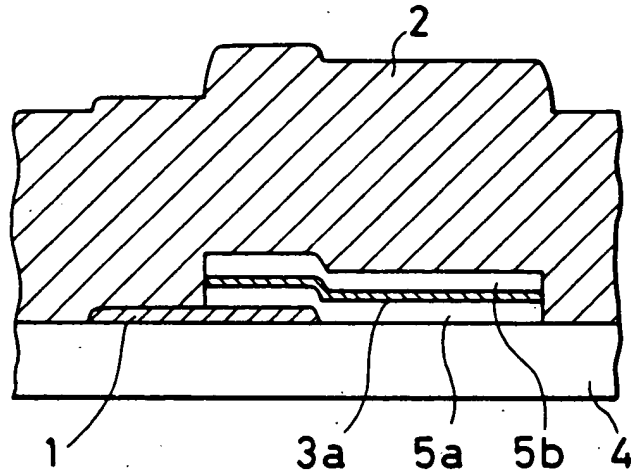
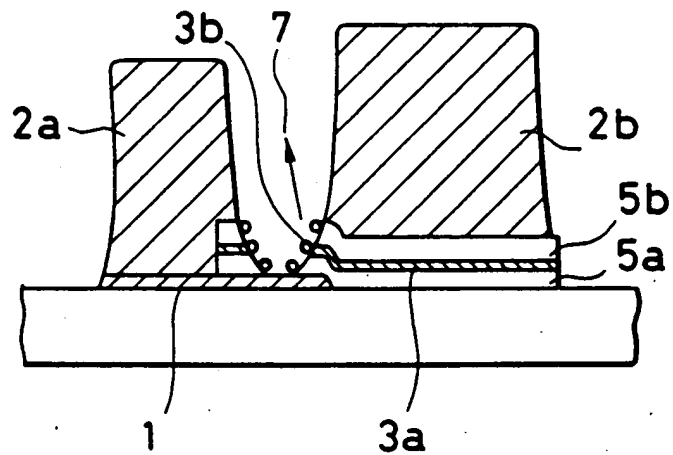


FIG.32B



APPROVED BY DRAFTSMAN	O.G. FIG.	
	CLASS	SUBCLASS

FIG.33A

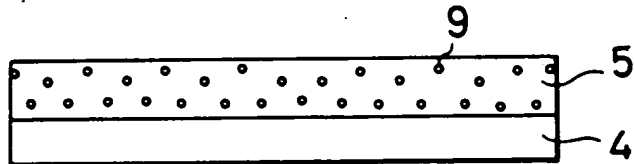


FIG.33B

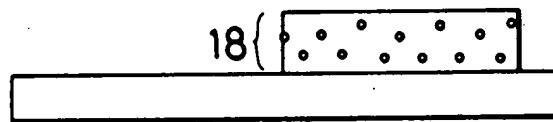


FIG.33C

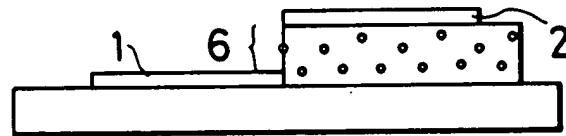
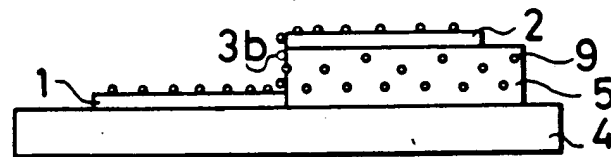


FIG.33D



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FIG.34A

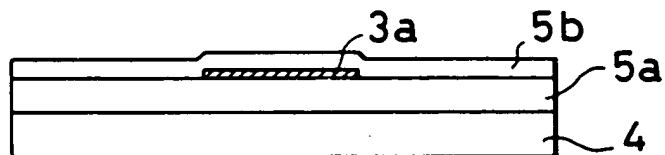


FIG.34B

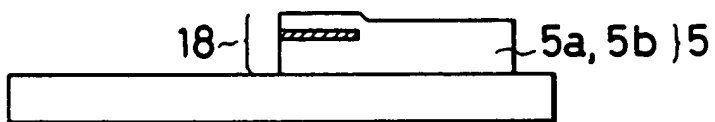


FIG.34C

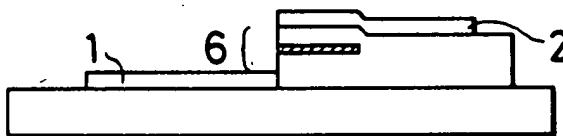
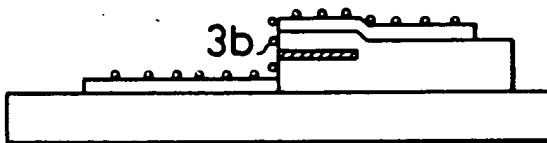


FIG.34D



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FIG.37A

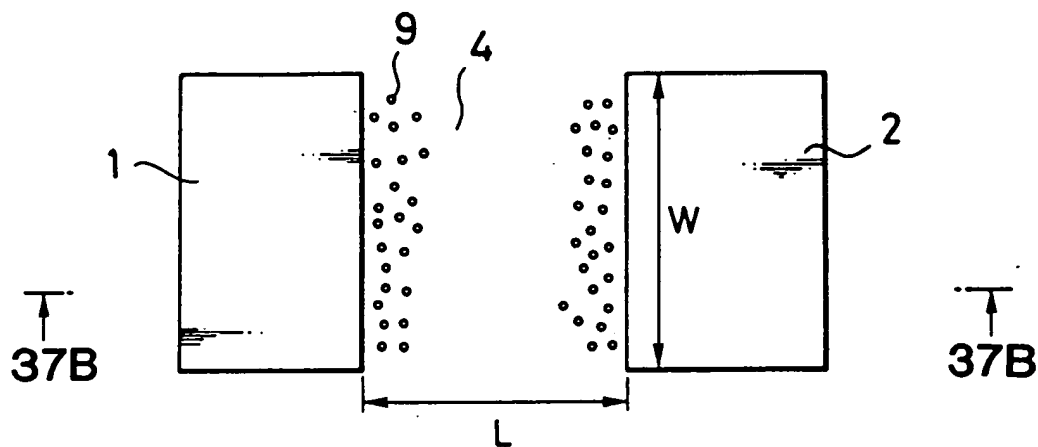


FIG.37B

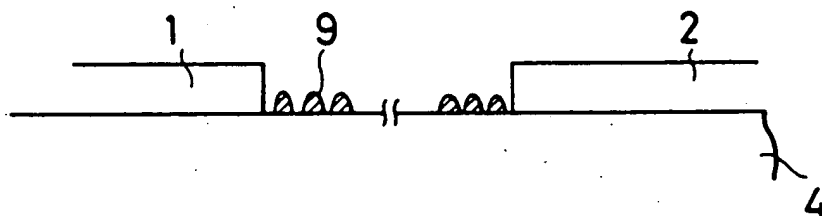
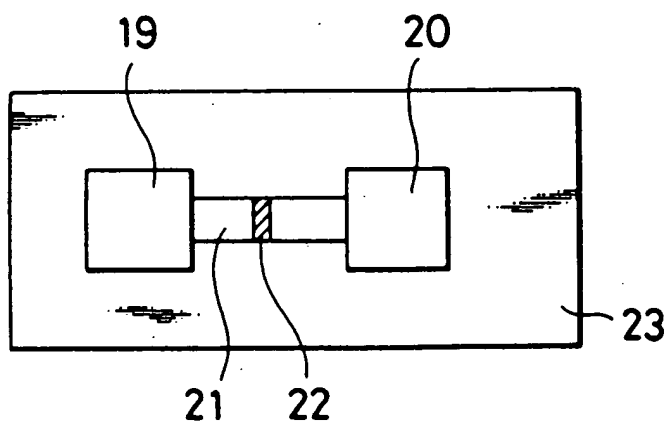


FIG.38



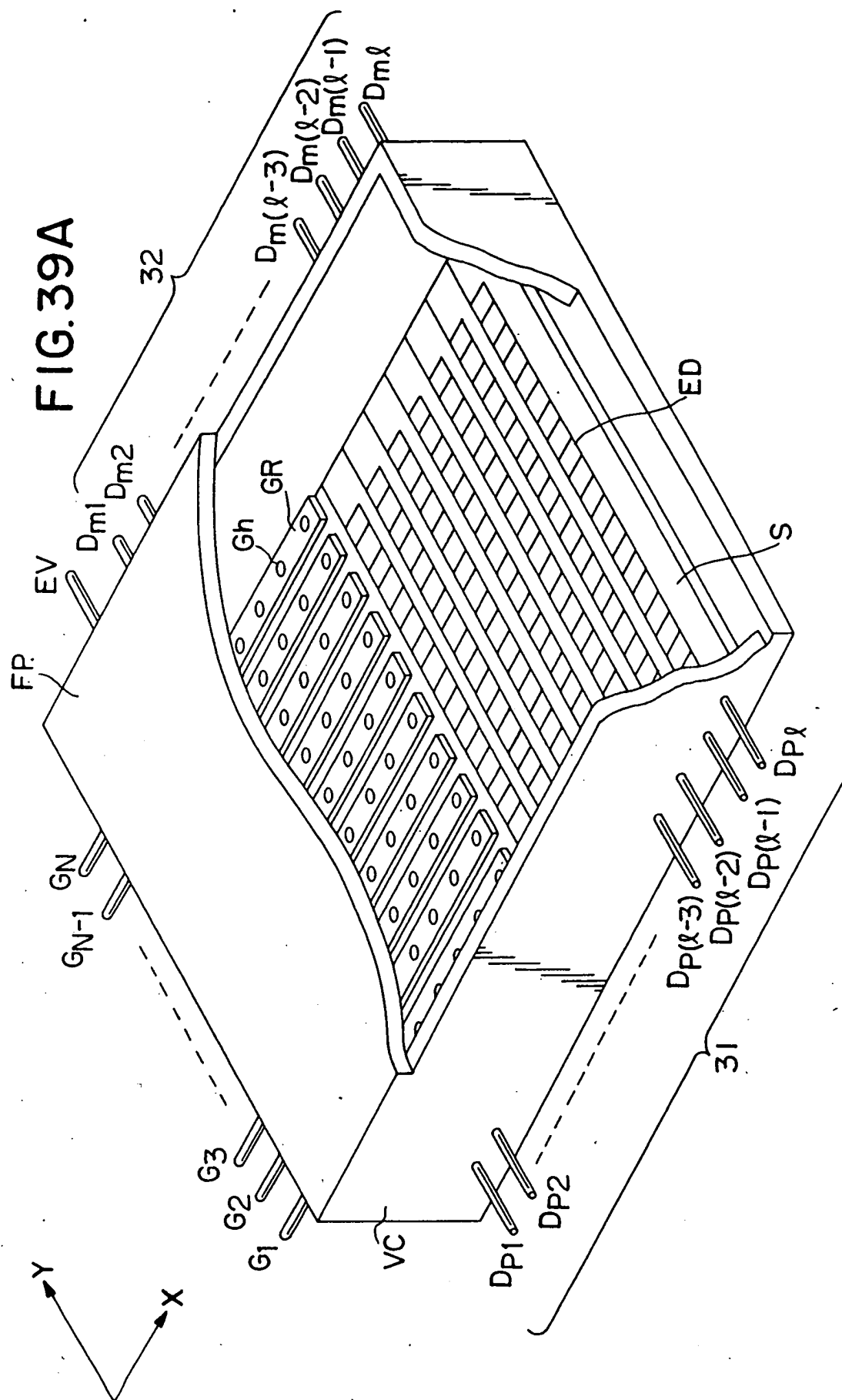
[illegible]

FIG. 39B

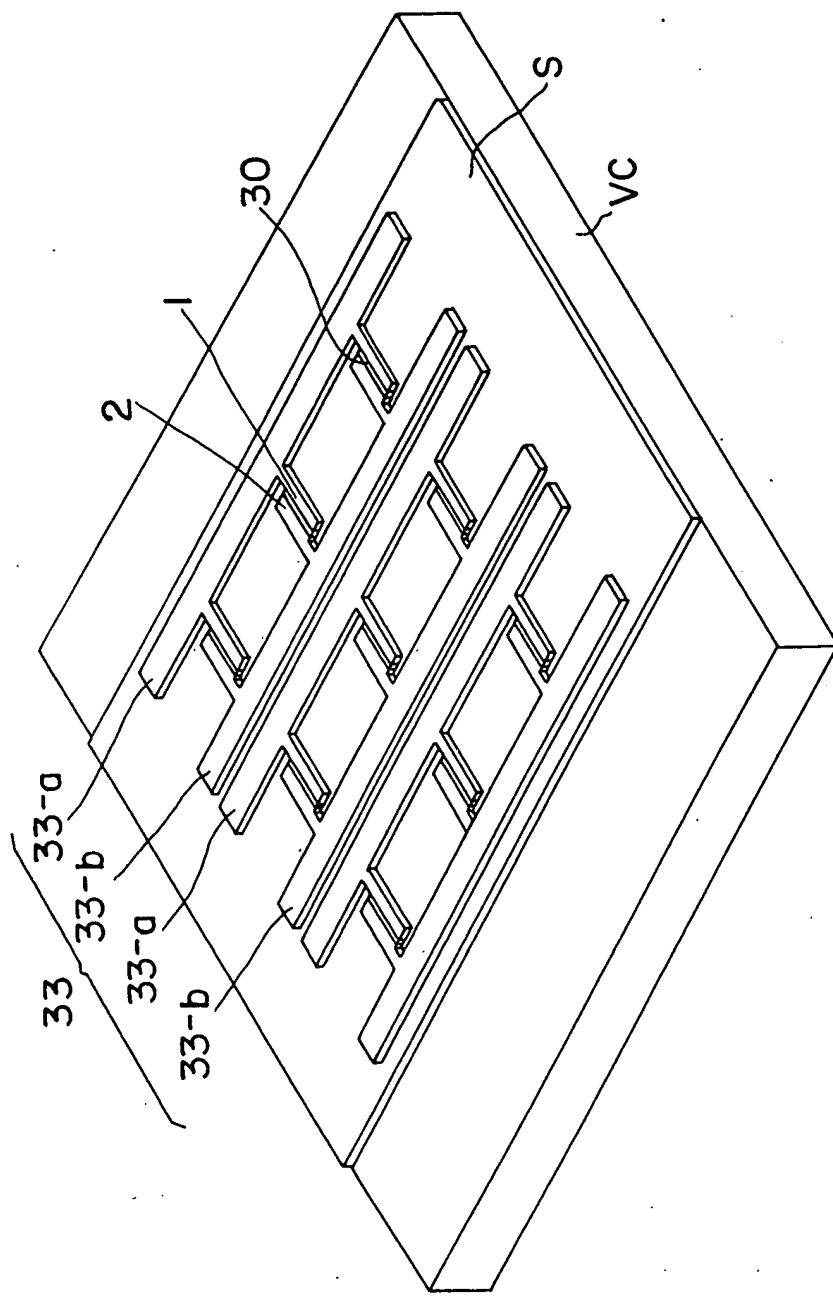


FIG. 39C

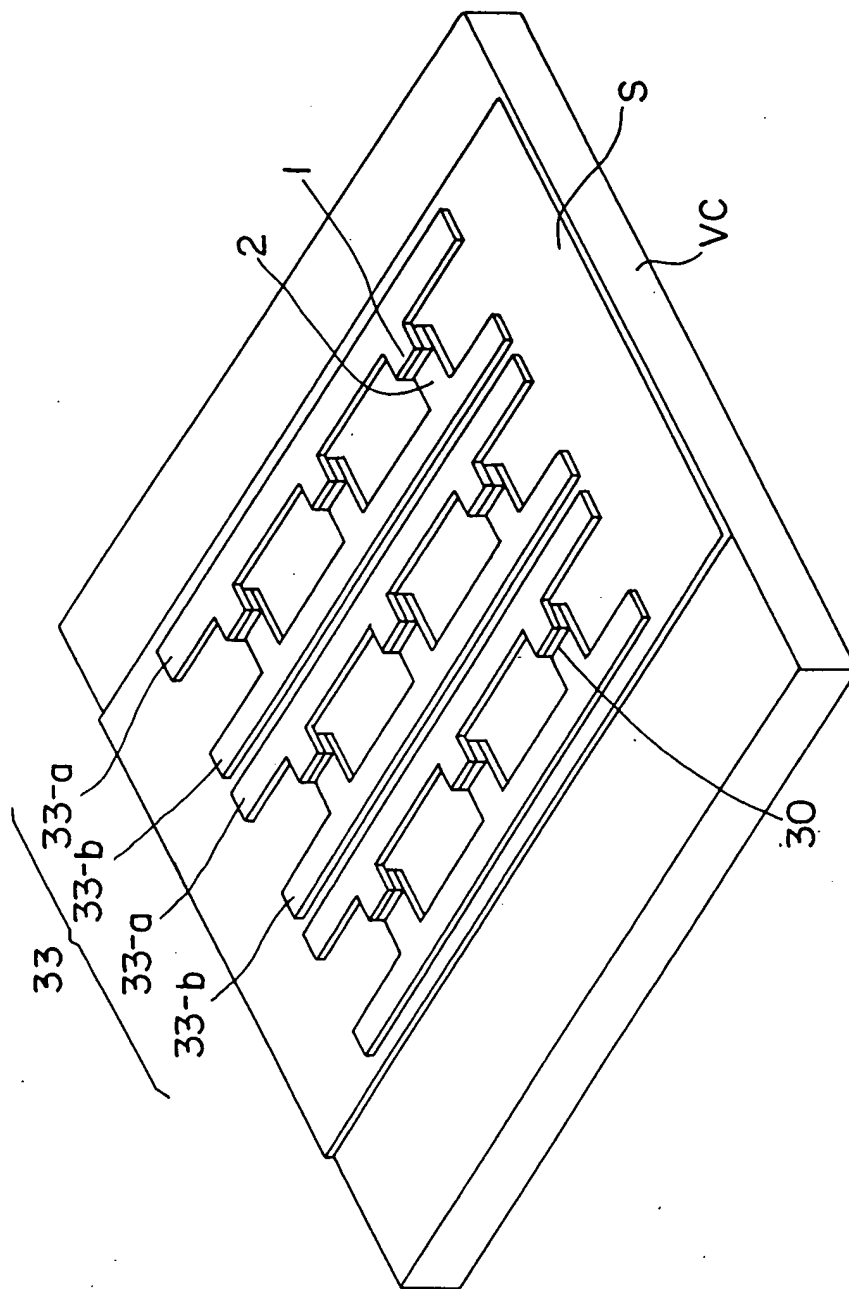


FIG. 39D

FIG. 39D is a perspective view of a semiconductor device. The device features a substrate with a grid of conductive lines (G1, G2, G3, GN-1, GN) and a series of conductive pads (Dm1, Dm2, Dm(l-3), Dm(l-2), Dm(l-1), Dm l). A central region is labeled ED. A dashed line indicates a cross-section line LA. Other labels include FP, EV, VC, TE, FL, DP1, DP2, DP(l-3), DP(l-2), DP(l-1), DP l, and S.

